MCP601/1R/2/3/4

2.7V to 6.0V Single Supply CMOS Op Amps

Features

- Single-Supply: 2.7V to 6.0V
- Rail-to-Rail Output
- Input Range Includes Ground
- Gain Bandwidth Product: 2.8 MHz (typical)
- Unity-Gain Stable
- Low Quiescent Current: 230 µA/amplifier (typical)
- Chip Select ($\overline{CS}$): **MCP603 only**
- Temperature Ranges:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C
- Available in Single, Dual, and Quad

Typical Applications

- Portable Equipment
- A/D Converter Driver
- Photo Diode Pre-amp
- Analog Filters
- Data Acquisition
- Notebooks and PDAs
- Sensor Interface

Available Tools

- SPICE Macro Models
- FilterLab® Software
- Mindi™ Simulation Tool
- MAPS (Microchip Advanced Part Selector)
- Analog Demonstration and Evaluation Boards
- Application Notes

Description

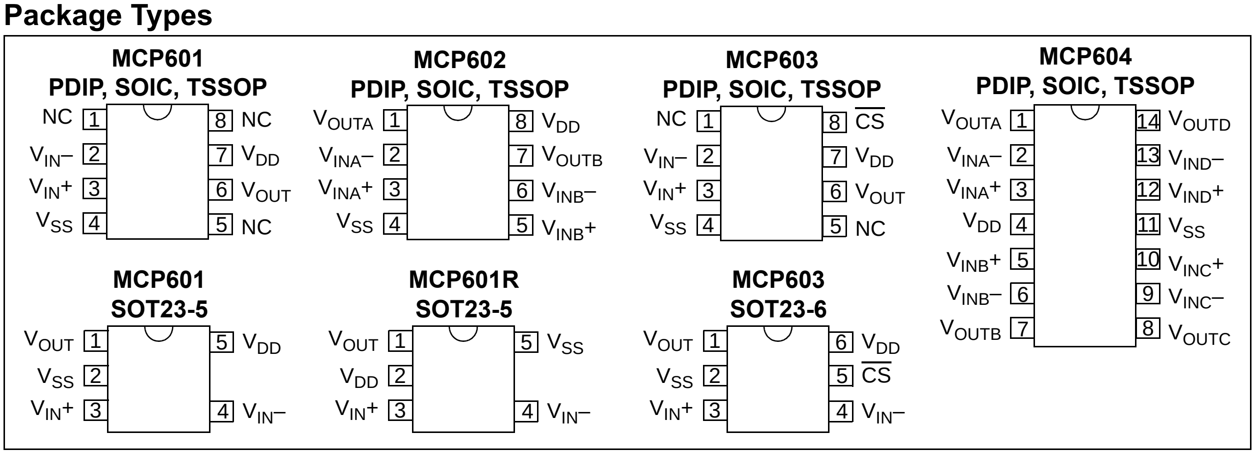
The Microchip Technology Inc. MCP601/1R/2/3/4 family of low-power operational amplifiers (op amps) are offered in single (MCP601), single with Chip Select ($\overline{CS}$) (MCP603), dual (MCP602), and quad (MCP604) configurations. These op amps utilize an advanced CMOS technology that provides low bias current, high-speed operation, high open-loop gain, and rail-to-rail output swing. This product offering operates with a single supply voltage that can be as low as 2.7V, while drawing 230 µA (typical) of quiescent current per amplifier. In addition, the common mode input voltage range goes 0.3V below ground, making these amplifiers ideal for single-supply operation.

These devices are appropriate for low power, battery operated circuits due to the low quiescent current, for A/D convert driver amplifiers because of their wide bandwidth or for anti-aliasing filters by virtue of their low input bias current.

The MCP601, MCP602, and MCP603 are available in standard 8-lead PDIP, SOIC, and TSSOP packages. The MCP601 and MCP601R are also available in a standard 5-lead SOT-23 package, while the MCP603 is available in a standard 6-lead SOT-23 package. The MCP604 is offered in standard 14-lead PDIP, SOIC, and TSSOP packages.

The MCP601/1R/2/3/4 family is available in the Industrial and Extended temperature ranges and has a power supply range of 2.7V to 6.0V.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} – V_{SS}$ 7.0V

Current at Input Pins ....±2 mA

Analog Inputs (V_{IN}+, V_{IN}–) †† .... V_{SS} – 1.0V to V_{DD} + 1.0V

All Other Inputs and Outputs .... V_{SS} – 0.3V to V_{DD} + 0.3V

Difference Input Voltage .... $|V_{DD} – V_{SS}|$

Output Short Circuit Current ....Continuous

Current at Output and Supply Pins ....±30 mA

Storage Temperature....................................–65°C to +150°C

Maximum Junction Temperature (T_J).........................+150°C

ESD Protection On All Pins (HBM; MM) .... ≥ 3 kV; 200V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage and Current Limits"**.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, and R_L = 100 kΩ to V_L, and $\overline{CS}$ is tied low. (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-2	±0.7	+2	mV	
Industrial Temperature	V_{OS}	-3	±1	+3	mV	T_A = -40°C to +85°C **(Note 1)**
Extended Temperature	V_{OS}	-4.5	±1	+4.5	mV	T_A = -40°C to +125°C **(Note 1)**
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	±2.5	—	µV/°C	T_A = -40°C to +125°C
Power Supply Rejection	PSRR	80	88	—	dB	V_{DD} = 2.7V to 5.5V
Input Current and Impedance						
Input Bias Current	I_B	—	1	—	pA	
Industrial Temperature	I_B	—	20	60	pA	T_A = +85°C **(Note 1)**
Extended Temperature	I_B	—	450	5000	pA	T_A = +125°C **(Note 1)**
Input Offset Current	I_{OS}	—	±1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}‖6	—	Ω‖pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}‖3	—	Ω‖pF	
Common Mode						
Common Mode Input Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} – 1.2	V	
Common Mode Rejection Ratio	CMRR	75	90	—	dB	V_{DD} = 5.0V, V_{CM} = -0.3V to 3.8V
Open-loop Gain						
DC Open-loop Gain (large signal)	A_{OL}	100	115	—	dB	R_L = 25 kΩ to V_L, V_{OUT} = 0.1V to V_{DD} – 0.1V
	A_{OL}	95	110	—	dB	R_L = 5 kΩ to V_L, V_{OUT} = 0.1V to V_{DD} – 0.1V
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 15	—	V_{DD} – 20	mV	R_L = 25 kΩ to V_L, Output overdrive = 0.5V
	V_{OL}, V_{OH}	V_{SS} + 45	—	V_{DD} – 60	mV	R_L = 5 kΩ to V_L, Output overdrive = 0.5V
Linear Output Voltage Swing	V_{OUT}	V_{SS} + 100	—	V_{DD} – 100	mV	R_L = 25 kΩ to V_L, A_{OL} ≥ 100 dB
	V_{OUT}	V_{SS} + 100	—	V_{DD} – 100	mV	R_L = 5 kΩ to V_L, A_{OL} ≥ 95 dB
Output Short Circuit Current	I_{SC}	—	±22	—	mA	V_{DD} = 5.5V
	I_{SC}	—	±12	—	mA	V_{DD} = 2.7V
Power Supply						
Supply Voltage	V_{DD}	2.7	—	6.0	V	**(Note 2)**
Quiescent Current per Amplifier	I_Q	—	230	325	µA	I_O = 0

Note 1: These specifications are not tested in either the SOT-23 or TSSOP packages with date codes older than YYWW = 0408. In these cases, the minimum and maximum values are by design and characterization only.

2: All parts with date codes November 2007 and later have been screened to ensure operation at V_{DD}=6.0V. However, the other minimum and maximum specifications are measured at 1.4V and/or 5.5V.

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, and R_L = 100 kΩ to V_L, C_L = 50 pF, and $\overline{CS}$ is tied low. (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Frequency Response						
Gain Bandwidth Product	GBWP	—	2.8	—	MHz	
Phase Margin	PM	—	50	—	°	G = +1 V/V
Step Response						
Slew Rate	SR	—	2.3	—	V/µs	G = +1 V/V
Settling Time (0.01%)	t_{settle}	—	4.5	—	µs	G = +1 V/V, 3.8V step
Noise						
Input Noise Voltage	E_{ni}	—	7	—	$µV_{P-P}$	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	29	—	nV/√Hz	f = 1 kHz
	e_{ni}	—	21	—	nV/√Hz	f = 10 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz

MCP603 CHIP SELECT ($\overline{CS}$) CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, and R_L = 100 kΩ to V_L, C_L = 50 pF, and $\overline{CS}$ is tied low. (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	-1.0	—	—	µA	$\overline{CS}$ = 0.2V_{DD}
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	0.7	2.0	µA	$\overline{CS}$ = V_{DD}
Shutdown V_{SS} current	I_{Q_SHDN}	-2.0	-0.7	—	µA	$\overline{CS}$ = V_{DD}
Amplifier Output Leakage in Shutdown	I_{O_SHDN}	—	1	—	nA	
Timing						
$\overline{CS}$ Low to Amplifier Output Turn-on Time	t_{ON}	—	3.1	10	µs	$\overline{CS} \le 0.2V_{DD}$, G = +1 V/V
$\overline{CS}$ High to Amplifier Output High-Z Time	t_{OFF}	—	100	—	ns	$\overline{CS} \ge 0.8V_{DD}$, G = +1 V/V, No load.
Hysteresis	V_{HYST}	—	0.4	—	V	V_{DD} = 5.0V

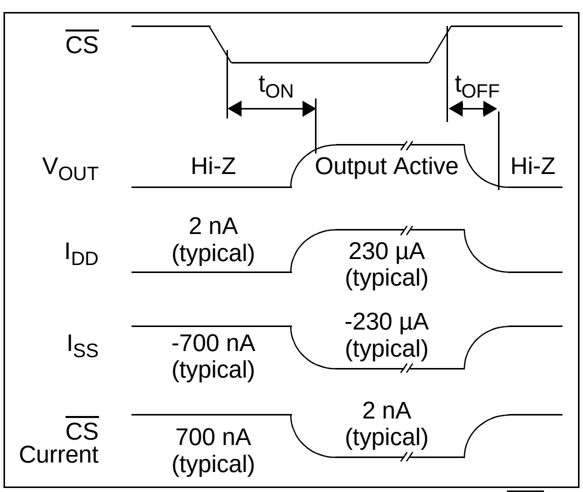


FIGURE 1-1: *MCP603 Chip Select ($\overline{CS}$) Timing Diagram.*

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	Industrial temperature parts
	T_A	-40	—	+125	°C	Extended temperature parts
Operating Temperature Range	T_A	-40	—	+125	°C	**Note**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 6L-SOT23	θ_{JA}	—	230	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-TSSOP	θ_{JA}	—	124	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note: The Industrial temperature parts operate over this extended range, but with reduced performance. The Extended temperature specs do not apply to Industrial temperature parts. In any case, the internal Junction temperature (T_J) must not exceed the absolute maximum specification of 150°C.

1.1 Test Circuits

The test circuits used for the DC and AC tests are shown in Figure 1-2 and Figure 1-2. The bypass capacitors are laid out according to the rules discussed in **Section 4.5 “Supply Bypass”**.

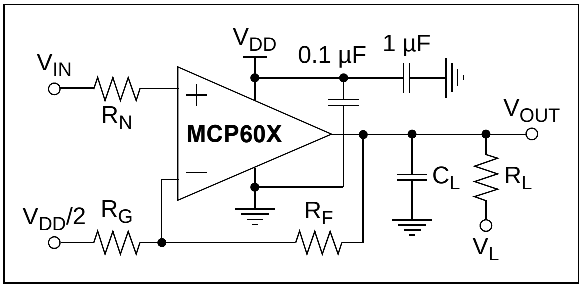


FIGURE 1-2: *AC and DC Test Circuit for Most Non-Inverting Gain Conditions.*

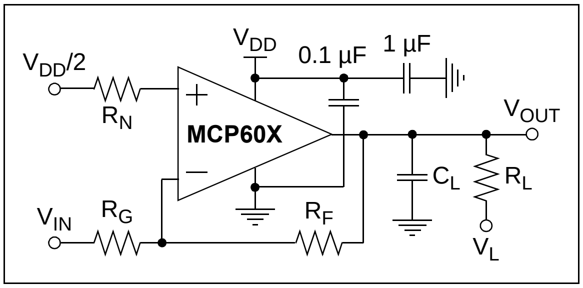


FIGURE 1-3: *AC and DC Test Circuit for Most Inverting Gain Conditions.*

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 100 kΩ to V_L, C_L = 50 pF and $\overline{CS}$ is tied low.

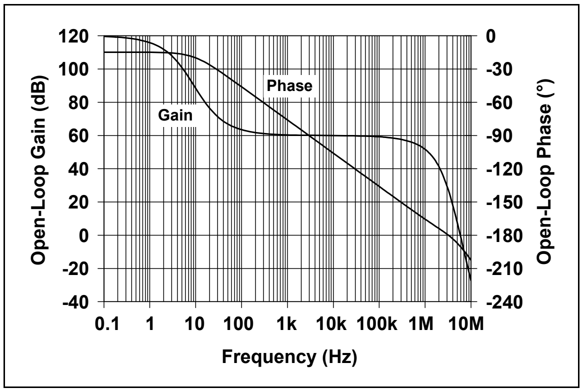


FIGURE 2-1: *Open-Loop Gain, Phase vs. Frequency.*

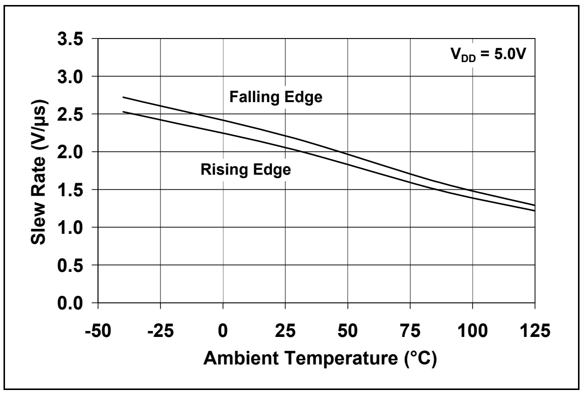


FIGURE 2-2: *Slew Rate vs. Temperature.*

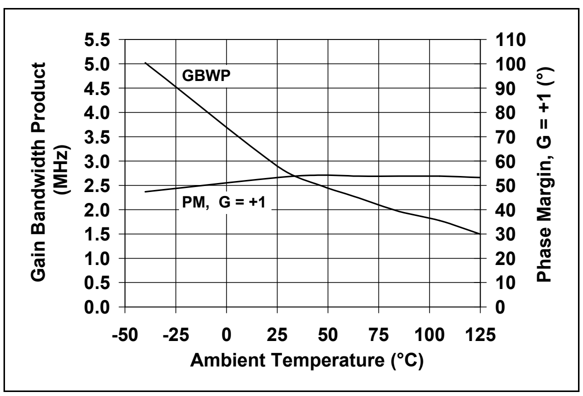


FIGURE 2-3: *Gain Bandwidth Product, Phase Margin vs. Temperature.*

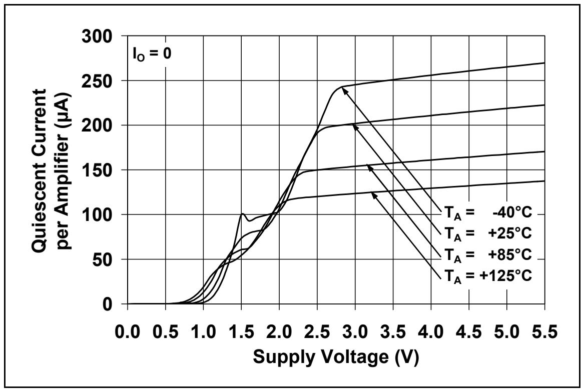


FIGURE 2-4: *Quiescent Current vs. Supply Voltage.*

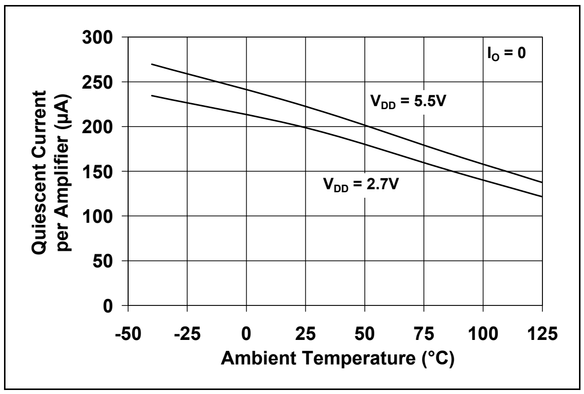


FIGURE 2-5: *Quiescent Current vs. Temperature.*

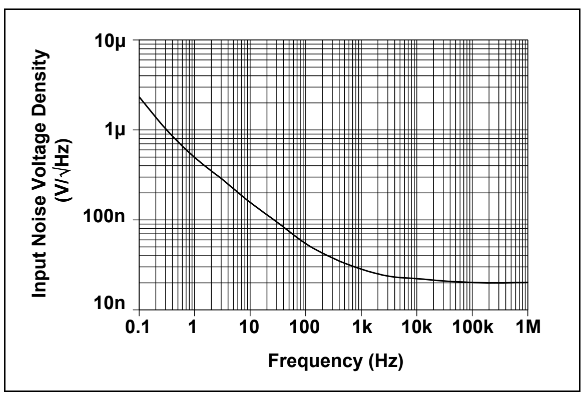


FIGURE 2-6: *Input Noise Voltage Density vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L, C_L = 50 pF and $\overline{CS}$ is tied low.

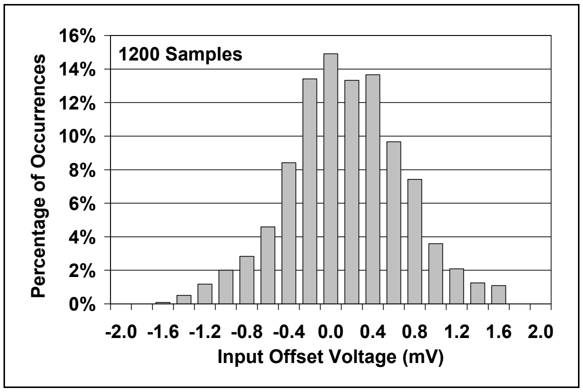


FIGURE 2-7: Input Offset Voltage.

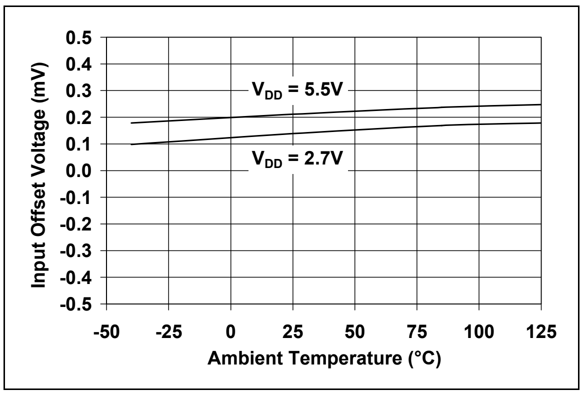


FIGURE 2-8: Input Offset Voltage vs. Temperature.

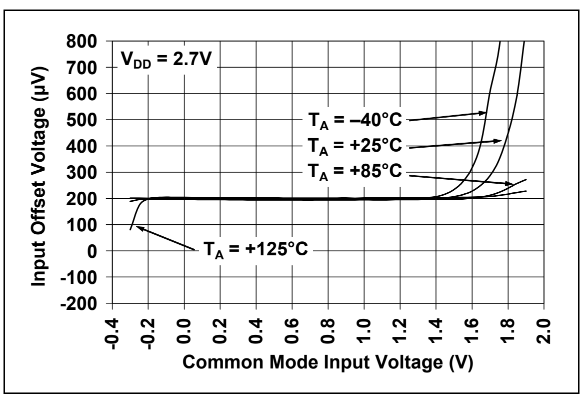


FIGURE 2-9: Input Offset Voltage vs. Common Mode Input Voltage with V_{DD} = 2.7V.

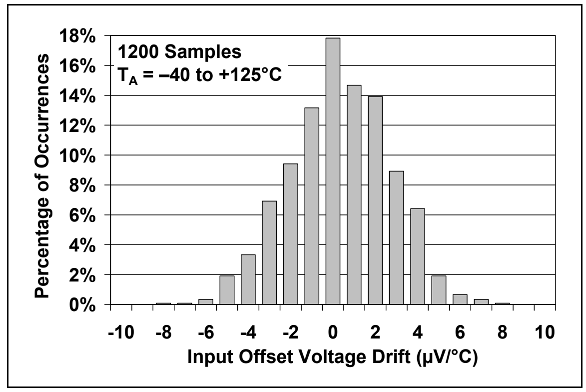


FIGURE 2-10: Input Offset Voltage Drift.

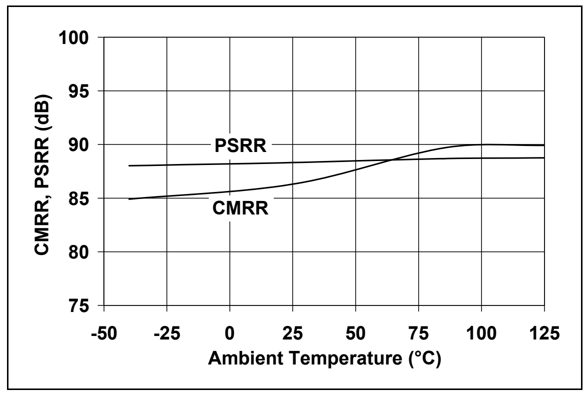


FIGURE 2-11: CMRR, PSRR vs. Temperature.

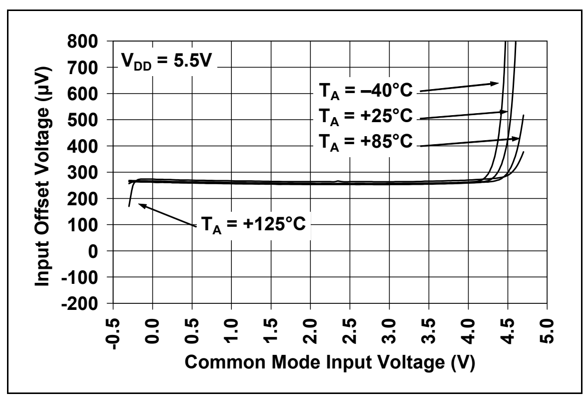


FIGURE 2-12: Input Offset Voltage vs. Common Mode Input Voltage with V_{DD} = 5.5V.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L, C_L = 50 pF and $\overline{CS}$ is tied low.

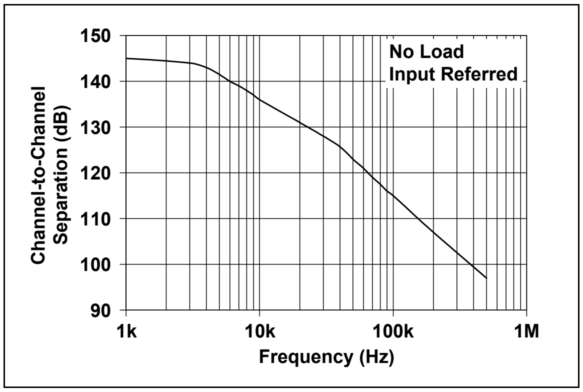


FIGURE 2-13: *Channel-to-Channel Separation vs. Frequency.*

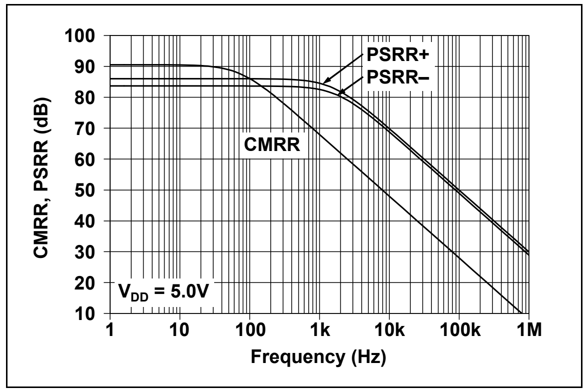


FIGURE 2-16: *CMRR, PSRR vs. Frequency.*

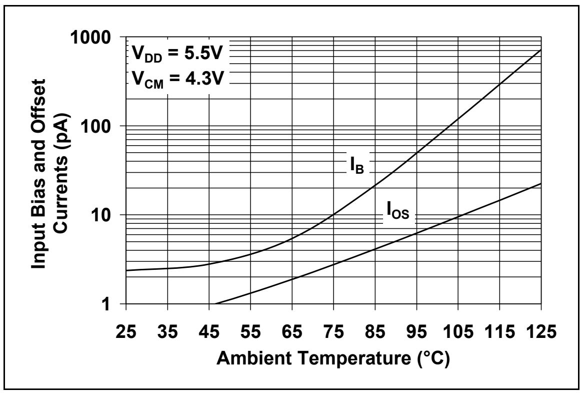


FIGURE 2-14: *Input Bias Current, Input Offset Current vs. Ambient Temperature.*

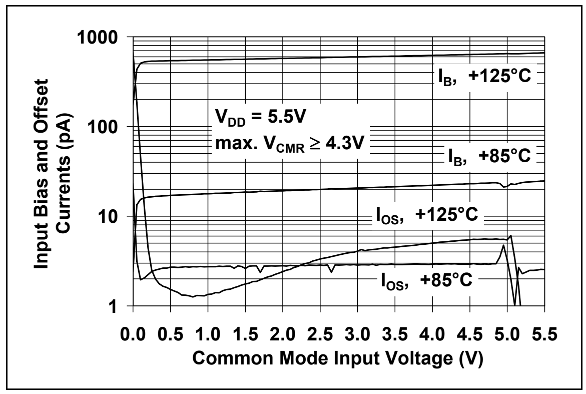


FIGURE 2-17: *Input Bias Current, Input Offset Current vs. Common Mode Input Voltage.*

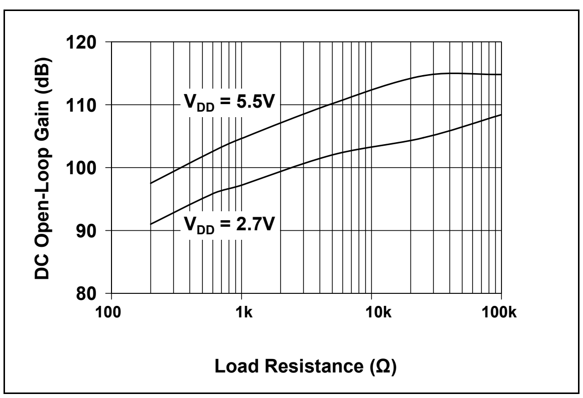


FIGURE 2-15: *DC Open-Loop Gain vs. Load Resistance.*

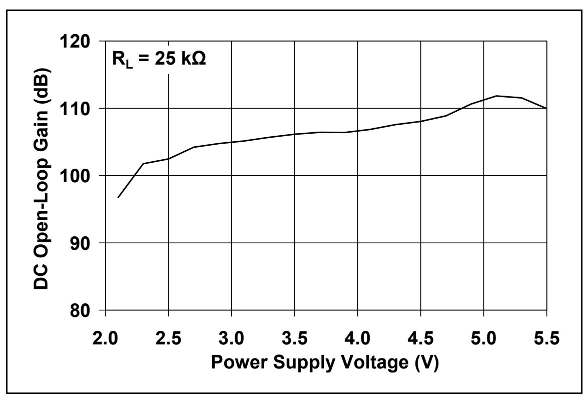


FIGURE 2-18: *DC Open-Loop Gain vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 100 kΩ to V_L, C_L = 50 pF and $\overline{CS}$ is tied low.

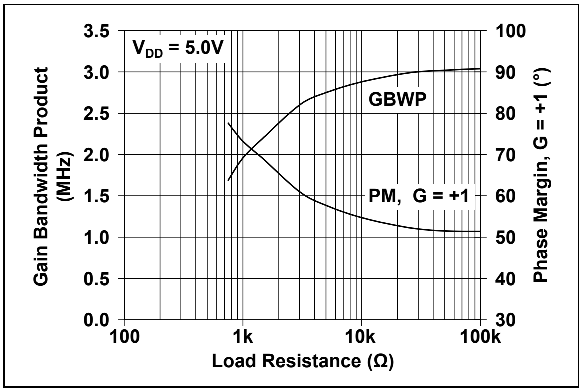


FIGURE 2-19: Gain Bandwidth Product, Phase Margin vs. Load Resistance.

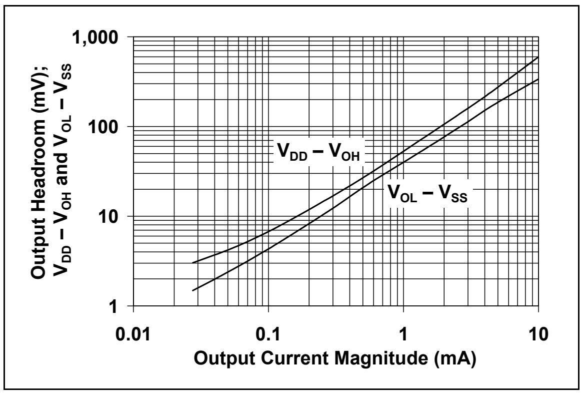


FIGURE 2-20: Output Voltage Headroom vs. Output Current.

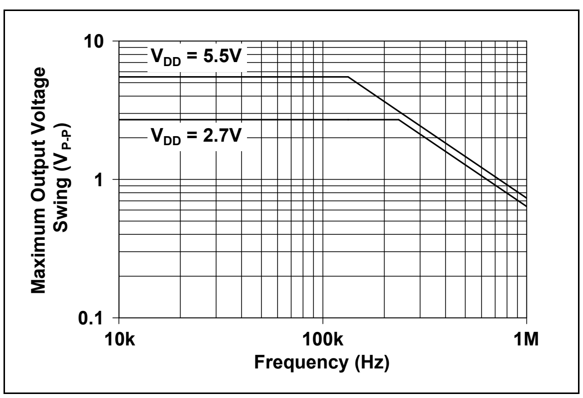


FIGURE 2-21: Maximum Output Voltage Swing vs. Frequency.

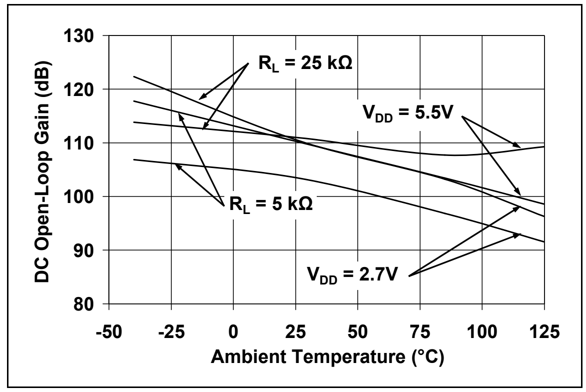


FIGURE 2-22: DC Open-Loop Gain vs. Temperature.

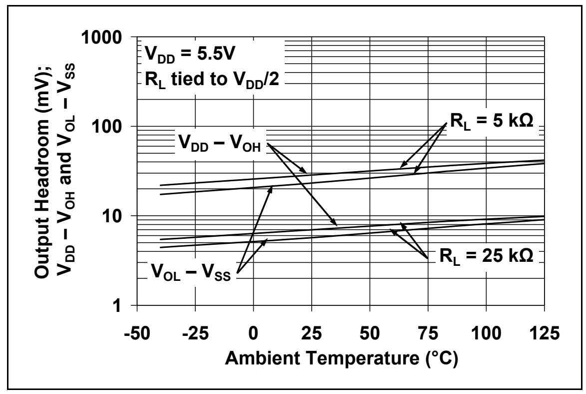


FIGURE 2-23: Output Voltage Headroom vs. Temperature.

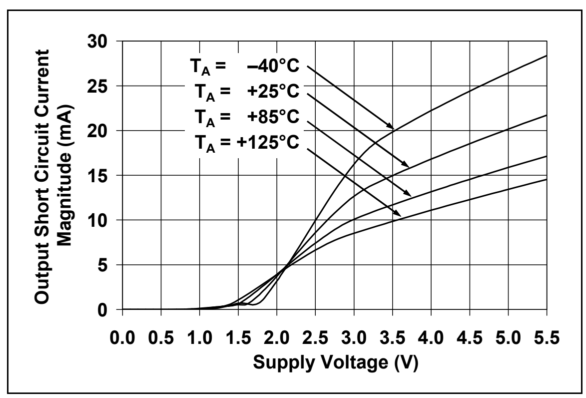


FIGURE 2-24: Output Short-Circuit Current vs. Supply Voltage.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L, C_L = 50 pF and $\overline{CS}$ is tied low.

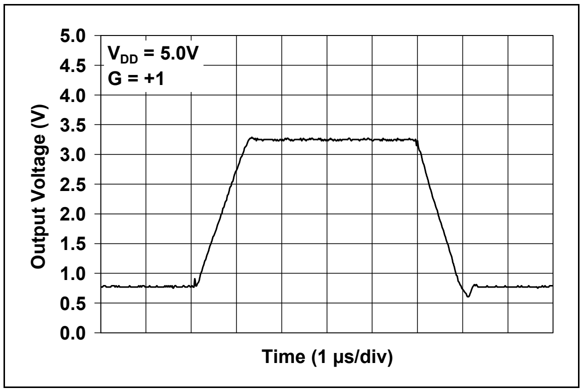


FIGURE 2-25: *Large Signal Non-Inverting Pulse Response.*

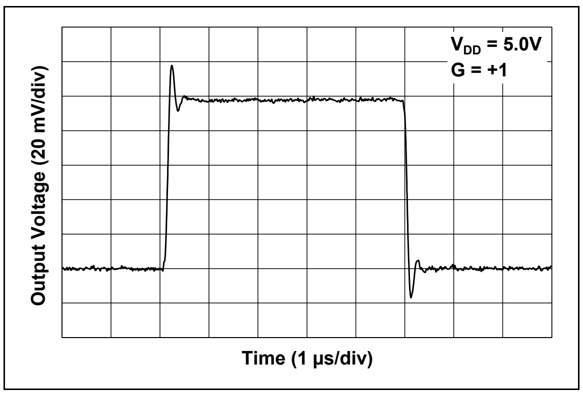


FIGURE 2-26: *Small Signal Non-Inverting Pulse Response.*

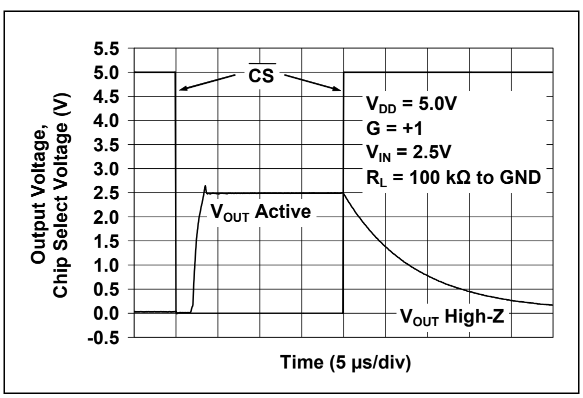


FIGURE 2-27: *Chip Select Timing (MCP603).*

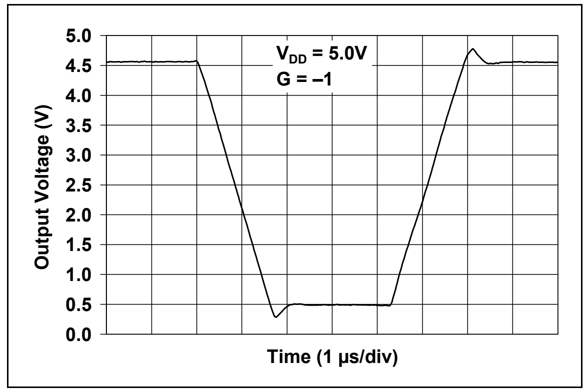


FIGURE 2-28: *Large Signal Inverting Pulse Response.*

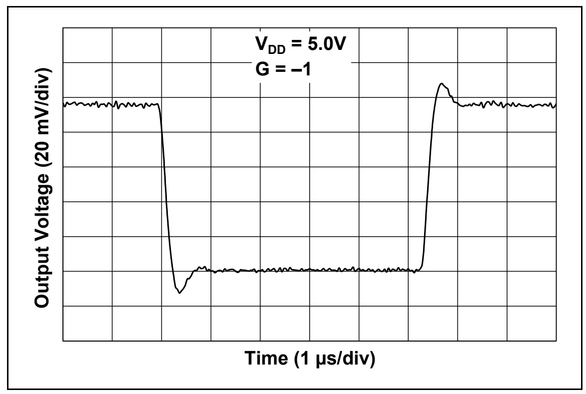


FIGURE 2-29: *Small Signal Inverting Pulse Response.*

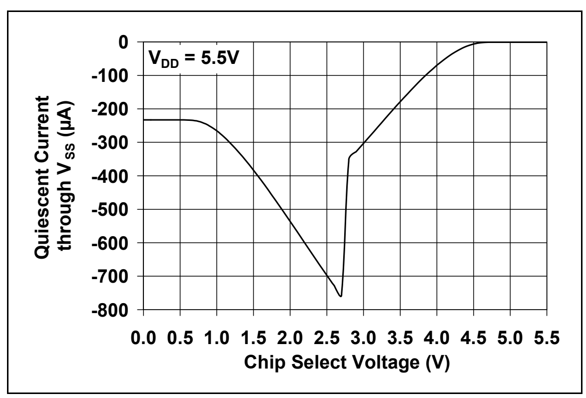


FIGURE 2-30: *Quiescent Current Through V_{SS} vs. Chip Select Voltage (MCP603).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 100 kΩ to V_L, C_L = 50 pF and $\overline{CS}$ is tied low.

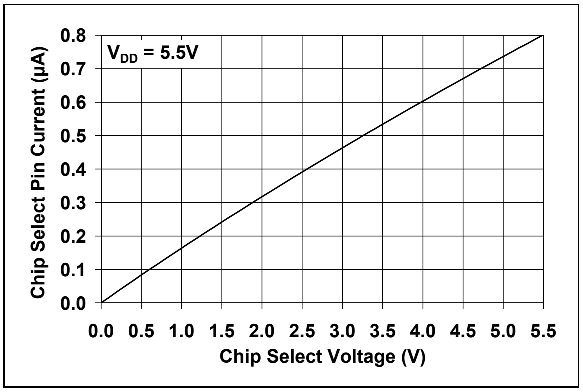


FIGURE 2-31: *Chip Select Pin Input Current vs. Chip Select Voltage.*

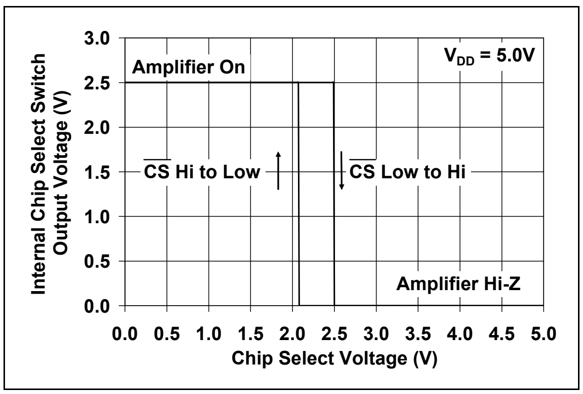


FIGURE 2-32: *Hysteresis of Chip Select's Internal Switch.*

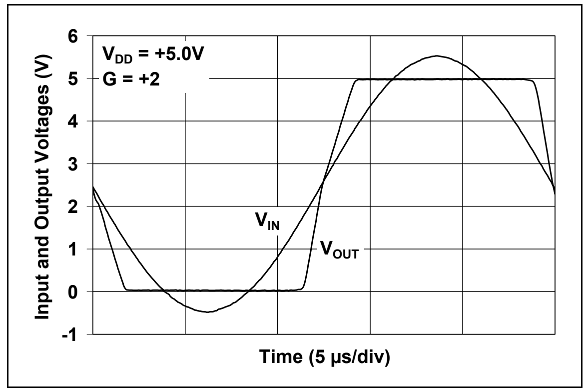


FIGURE 2-33: *The MCP601/1R/2/3/4 family of op amps shows no phase reversal under input overdrive.*

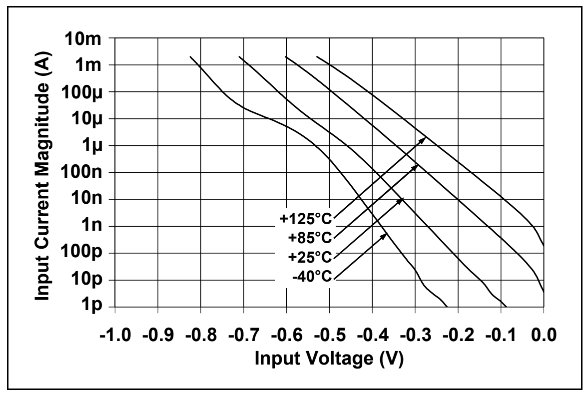


FIGURE 2-34: *Measured Input Current vs. Input Voltage (below V_{SS}).*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1 (single op amps) and Table 3-2 (dual and quad op amps).

TABLE 3-1: PIN FUNCTION TABLE FOR SINGLE OP AMPS

MCP601		MCP601R	MCP603		Symbol	Description
PDIP, SOIC, TSSOP	SOT-23-5	SOT-23-5 **(Note 1)**	SOT-23-6	PDIP, SOIC, TSSOP		
6	1	1	6	6	V_{OUT}	Analog Output
2	4	4	2	2	$V_{IN}-$	Inverting Input
3	3	3	3	3	$V_{IN}+$	Non-inverting Input
7	5	2	7	7	V_{DD}	Positive Power Supply
4	2	5	4	4	V_{SS}	Negative Power Supply
—	—	—	8	8	$\overline{CS}$	Chip Select
1, 5, 8	—	—	1, 5	1	NC	No Internal Connection

Note 1: The MCP601R is only available in the 5-pin SOT-23 package.

TABLE 3-2: PIN FUNCTION TABLE FOR DUAL AND QUAD OP AMPS

MCP602	MCP604	Symbol	Description
PDIP, SOIC, TSSOP	PDIP, SOIC, TSSOP		
1	1	V_{OUTA}	Analog Output (op amp A)
2	2	$V_{INA}-$	Inverting Input (op amp A)
3	3	$V_{INA}+$	Non-inverting Input (op amp A)
8	4	V_{DD}	Positive Power Supply
5	5	$V_{INB}+$	Non-inverting Input (op amp B)
6	6	$V_{INB}-$	Inverting Input (op amp B)
7	7	V_{OUTB}	Analog Output (op amp B)
—	8	V_{OUTC}	Analog Output (op amp C)
—	9	$V_{INC}-$	Inverting Input (op amp C)
—	10	$V_{INC}+$	Non-inverting Input (op amp C)
4	11	V_{SS}	Negative Power Supply
—	12	$V_{IND}+$	Non-inverting Input (op amp D)
—	13	$V_{IND}-$	Inverting Input (op amp D)
—	14	V_{OUTD}	Analog Output (op amp D)

3.1 Analog Outputs

The op amp output pins are low-impedance voltage sources.

3.2 Analog Inputs

The op amp non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Chip Select Digital Input

This is a CMOS, Schmitt-triggered input that places the part into a low power mode of operation.

3.4 Power Supply Pins

The positive power supply pin (V_{DD}) is 2.5V to 6.0V higher than the negative power supply pin (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

4.0 APPLICATIONS INFORMATION

The MCP601/1R/2/3/4 family of op amps are fabricated on Microchip's state-of-the-art CMOS process. They are unity-gain stable and suitable for a wide range of general purpose applications.

4.1 Inputs

4.1.1 PHASE REVERSAL

The MCP601/1R/2/3/4 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-34 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

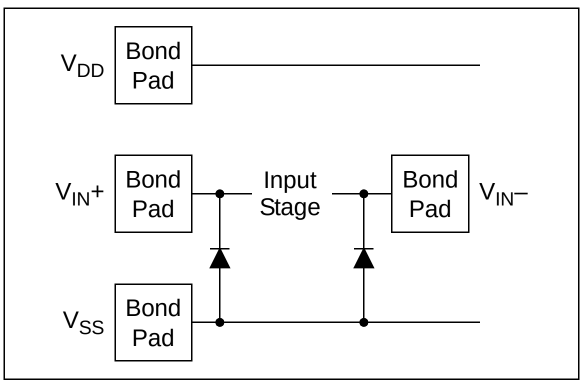
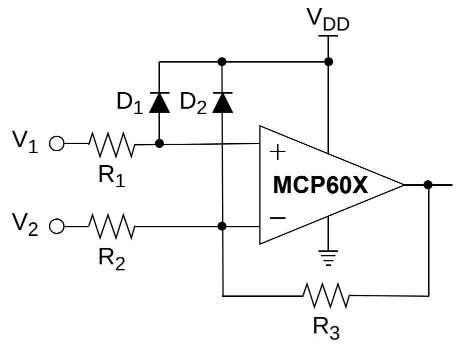


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the currents and voltages at the $V_{IN}+$ and $V_{IN}-$ pins (see **Absolute Maximum Ratings †** at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins ($V_{IN}+$ and $V_{IN}-$) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins ($V_{IN}+$ and $V_{IN}-$) from going too far above V_{DD}, and dump any currents onto V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.



$$R_1 > \frac{V_{SS} - (\text{minimum expected } V_1)}{2\ mA}$$

$$R_2 > \frac{V_{SS} - (\text{minimum expected } V_2)}{2\ mA}$$

FIGURE 4-2: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of resistors R_1 and R_2. In this case, current through the diodes D_1 and D_2 needs to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins ($V_{IN}+$ and $V_{IN}-$) should be very small.

A significant amount of current can flow out of the inputs when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-34. Applications that are high impedance may need to limit the useable voltage range.

4.1.3 NORMAL OPERATION

The Common Mode Input Voltage Range (V_{CMR}) includes ground in single-supply systems (V_{SS}), but does not include V_{DD}. This means that the amplifier input behaves linearly as long as the Common Mode Input Voltage (V_{CM}) is kept within the specified V_{CMR} limits (V_{SS}–0.3V to V_{DD}–1.2V at +25°C).

Figure 4-3 shows a unity gain buffer. Since V_{OUT} is the same voltage as the inverting input, V_{OUT} must be kept below V_{DD}–1.2V for correct operation.

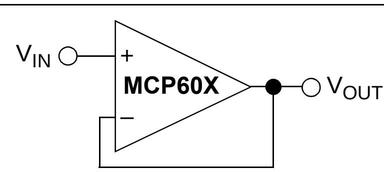


FIGURE 4-3: *Unity Gain Buffer has a Limited V_{OUT} Range.*

4.2 Rail-to-Rail Output

There are two specifications that describe the output swing capability of the MCP601/1R/2/3/4 family of op amps. The first specification (Maximum Output Voltage Swing) defines the absolute maximum swing that can be achieved under the specified load conditions. For instance, the output voltage swings to within 15 mV of the negative rail with a 25 kΩ load to $V_{DD}/2$. Figure 2-33 shows how the output voltage is limited when the input goes beyond the linear region of operation.

The second specification that describes the output swing capability of these amplifiers is the Linear Output Voltage Swing. This specification defines the maximum output swing that can be achieved while the amplifier is still operating in its linear region. To verify linear operation in this range, the large signal (DC Open-Loop Gain (A_{OL})) is measured at points 100 mV inside the supply rails. The measurement must exceed the specified gains in the specification table.

4.3 MCP603 Chip Select

The MCP603 is a single amplifier with Chip Select ($\overline{CS}$). When $\overline{CS}$ is pulled high, the supply current drops to -0.7 µA (typ.), which is pulled through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier output is put into a high-impedance state. Pulling $\overline{CS}$ low enables the amplifier.

The $\overline{CS}$ pin has an internal 5 MΩ (typical) pull-down resistor connected to V_{SS}, so it will go low if the $\overline{CS}$ pin is left floating. Figure 1-1 is the Chip Select timing diagram and shows the output voltage, supply currents, and $\overline{CS}$ current in response to a $\overline{CS}$ pulse. Figure 2-27 shows the measured output voltage response to a $\overline{CS}$ pulse.

4.4 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response with overshoot and ringing in the step response.

When driving large capacitive loads with these op amps (e.g., > 40 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-4) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

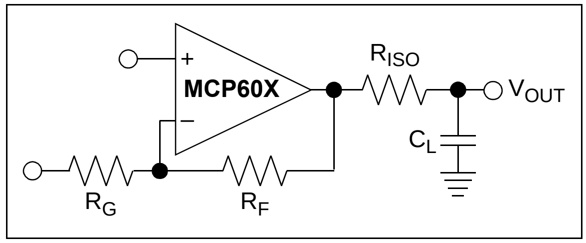


FIGURE 4-4: *Output resistor R_{ISO} stabilizes large capacitive loads.*

Figure 4-5 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N) in order to make it easier to interpret the plot for arbitrary gains. G_N is the circuit's noise gain. For non-inverting gains, G_N and the gain are equal. For inverting gains, G_N = 1 + |Gain| (e.g., -1 V/V gives G_N = +2 V/V).

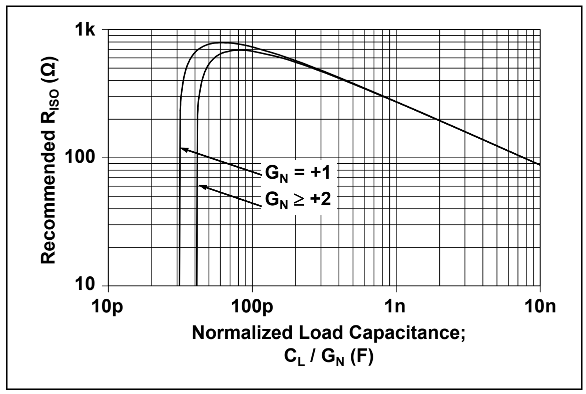


FIGURE 4-5: *Recommended R_{ISO} values for capacitive loads.*

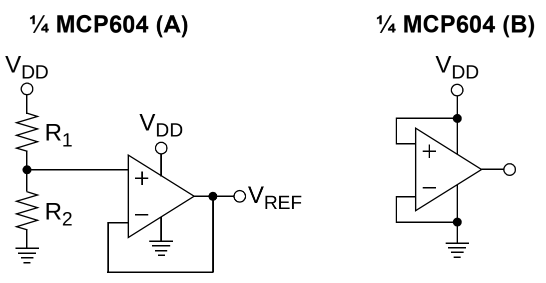
Once you have selected R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot in your circuit. Evaluation on the bench and simulations with the MCP601/1R/2/3/4 SPICE macro model are very helpful. Modify R_{ISO}'s value until the response is reasonable.

4.5 Supply Bypass

With this family of op amps, the power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with nearby analog parts.

4.6 Unused Op Amps

An unused op amp in a quad package (MCP604) should be configured as shown in Figure 4-6. These circuits prevent the output from toggling and causing crosstalk. Circuits A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.



$$V_{REF} = V_{DD} \cdot \frac{R_2}{R_1 + R_2}$$

FIGURE 4-6: *Unused Op Amps.*

4.7 PCB Surface Leakage

In applications where low input bias current is critical, printed circuit board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow. This is greater than the MCP601/1R/2/3/4 family's bias current at +25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-7.

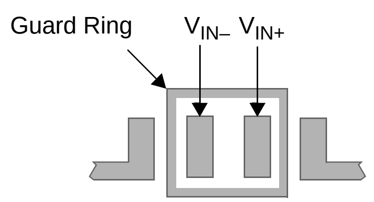


FIGURE 4-7: *Example Guard Ring layout.*

1. Connect the guard ring to the inverting input pin (V_{IN}–) for non-inverting gain amplifiers, including unity-gain buffers. This biases the guard ring to the common mode input voltage.
2. Connect the guard ring to the non-inverting input pin (V_{IN}+) for inverting gain amplifiers and transimpedance amplifiers (converts current to voltage, such as photo detectors). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).

4.8 Typical Applications

4.8.1 ANALOG FILTERS

Figure 4-8 and Figure 4-9 show low-pass, second-order, Butterworth filters with a cutoff frequency of 10 Hz. The filter in Figure 4-8 has a non-inverting gain of +1 V/V, and the filter in Figure 4-9 has an inverting gain of -1 V/V.

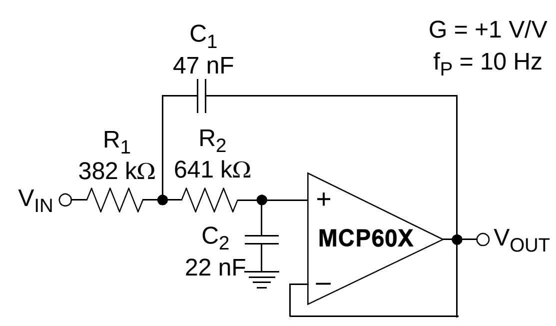


FIGURE 4-8: *Second-Order, Low-Pass Sallen-Key Filter.*

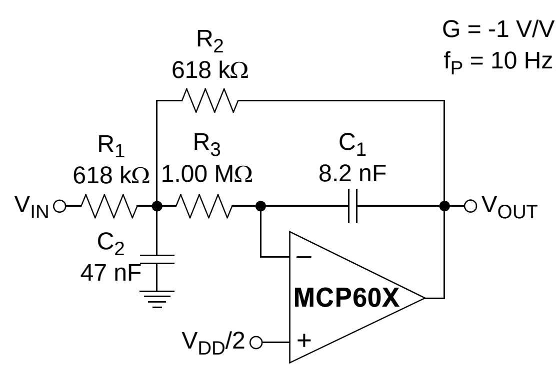


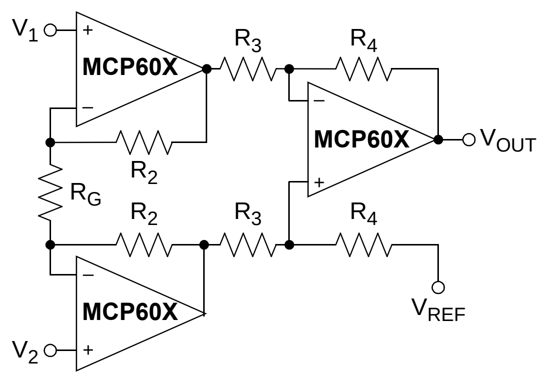
FIGURE 4-9: *Second-Order, Low-Pass Multiple-Feedback Filter.*

The MCP601/1R/2/3/4 family of op amps have low input bias current, which allows the designer to select larger resistor values and smaller capacitor values for these filters. This helps produce a compact PCB layout. These filters, and others, can be designed using Microchip's Design Aids; see **Section 5.2 "FilterLab® Software"** and **Section 5.3 "Mindi™ Simulatior Tool"**.

4.8.2 INSTRUMENTATION AMPLIFIER CIRCUITS

Instrumentation amplifiers have a differential input that subtracts one input voltage from another and rejects common mode signals. These amplifiers also provide a single-ended output voltage.

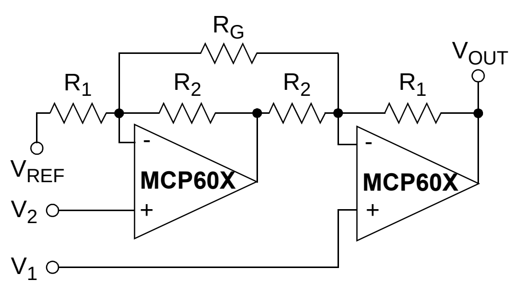
The three-op amp instrumentation amplifier is illustrated in Figure 4-10. One advantage of this approach is unity-gain operation, while one disadvantage is that the common mode input range is reduced as R_2/R_G gets larger.



$$V_{OUT} = (V_1 - V_2)\left(1 + \frac{2R_2}{R_G}\right)\left(\frac{R_4}{R_3}\right) + V_{REF}$$

FIGURE 4-10: *Three-Op Amp Instrumentation Amplifier.*

The two-op amp instrumentation amplifier is shown in Figure 4-11. While its power consumption is lower than the three-op amp version, its main drawbacks are that the common mode range is reduced with higher gains and it must be configured in gains of two or higher.



$$V_{OUT} = (V_1 - V_2)\left(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}\right) + V_{REF}$$

FIGURE 4-11: *Two-Op Amp Instrumentation Amplifier.*

Both instrumentation amplifiers should use a bulk bypass capacitor of at least 1 µF. The CMRR of these amplifiers will be set by both the op amp CMRR and resistor matching.

4.8.3 PHOTO DETECTION

The MCP601/1R/2/3/4 op amps can be used to easily convert the signal from a sensor that produces an output current (such as a photo diode) into a voltage (a transimpedance amplifier). This is implemented with a single resistor (R_2) in the feedback loop of the amplifiers shown in Figure 4-12 and Figure 4-13. The optional capacitor (C_2) sometimes provides stability for these circuits.

A photodiode configured in the Photovoltaic mode has zero voltage potential placed across it (Figure 4-12). In this mode, the light sensitivity and linearity is maximized, making it best suited for precision applications. The key amplifier specifications for this application are: low input bias current, low noise, common mode input voltage range (including ground), and rail-to-rail output.

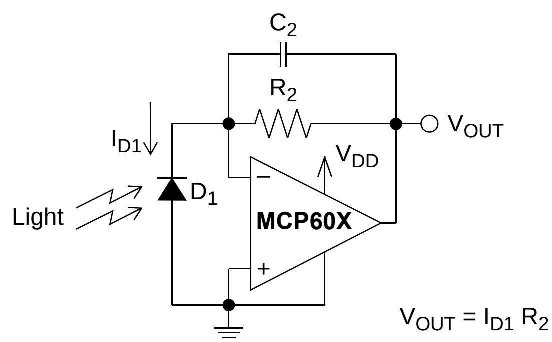


FIGURE 4-12: *Photovoltaic Mode Detector.*

In contrast, a photodiode that is configured in the Photoconductive mode has a reverse bias voltage across the photo-sensing element (Figure 4-13). This decreases the diode capacitance, which facilitates high-speed operation (e.g., high-speed digital communications). The design trade-off is increased diode leakage current and linearity errors. The op amp needs to have a wide Gain Bandwidth Product (GBWP).

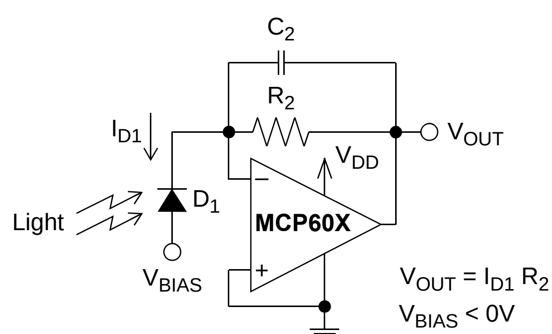


FIGURE 4-13: *Photoconductive Mode Detector.*

5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP601/1R/2/3/4 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP601/1R/2/3/4 op amps is available on the Microchip web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation over the temperature range. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Mindi™ Simulatior Tool

Microchip's Mindi™ simulator tool aids in the design of various circuits useful for active filter, amplifier and power-management applications. It is a free online simulation tool available from the Microchip web site at www.microchip.com/mindi. This interactive simulator enables designers to quickly generate circuit diagrams, simulate circuits. Circuits developed using the Mindi simulation tool can be downloaded to a personal computer or workstation.

5.4 MAPS (Microchip Advanced Part Selector)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparasion reports. Helpful links are also provided for Datasheets, Purchase, and Sampling of Microchip parts.

5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Two of our boards that are especially useful are:

- **P/N SOIC8EV:** *8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board*
- **P/N SOIC14EV:** *14-Pin SOIC/TSSOP/DIP Evaluation Board*

5.6 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip. com/appnotes and are recommended as supplemental reference resources.

ADN003: *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821

AN722: *"Operational Amplifier Topologies and DC Specifications",* DS00722

AN723: *"Operational Amplifier AC Specifications and Applications",* DS00723

AN884: *"Driving Capacitive Loads With Op Amps",* DS00884

AN990: *"Analog Sensor Conditioning Circuits – An Overview",* DS00990

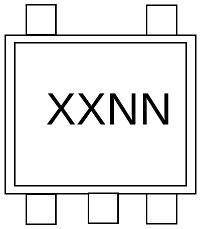
These application notes and others are listed in the design guide:

"Signal Chain Design Guide", DS21825

6.0 PACKAGING INFORMATION

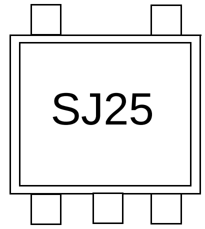
6.1 Package Marking Information

5-Lead SOT-23 (**MCP601 and MCP601R only**)

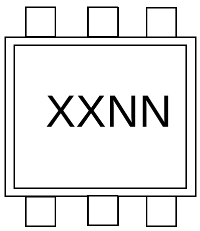


Device	I-Temp Code	E-Temp Code
MCP601	SANN	SLNN
MCP601R	SJNN	SMNN

Example:

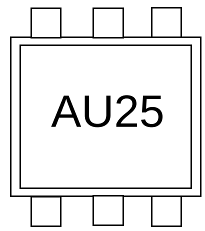


6-Lead SOT-23 (**MCP603 only)**



Device	I-Temp Code	E-Temp Code
MCP603	AENN	AUNN

Example:



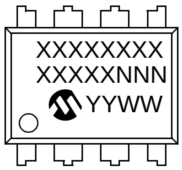
Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

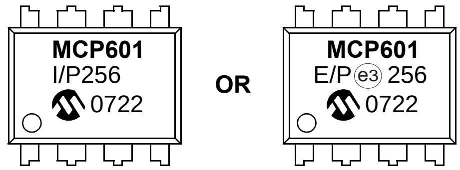
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

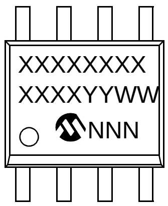
8-Lead PDIP (300 mil)



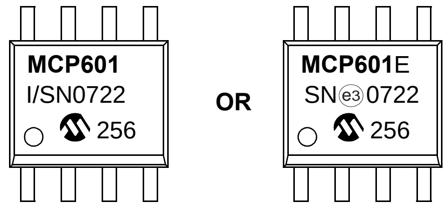
Example:



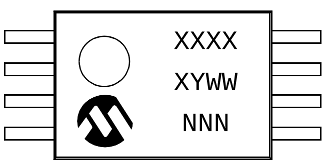
8-Lead SOIC (150 mil)



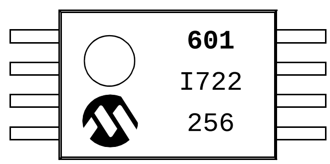
Example:



8-Lead TSSOP

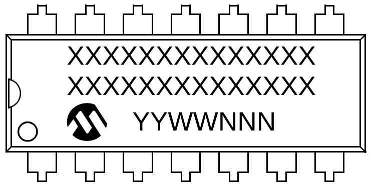


Example:

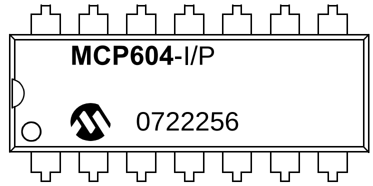


Package Marking Information (Continued)

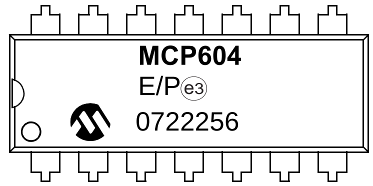
14-Lead PDIP (300 mil) (**MCP604**)



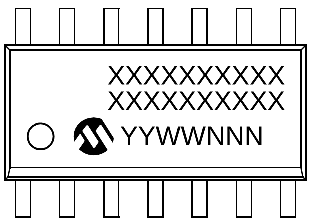
Example:



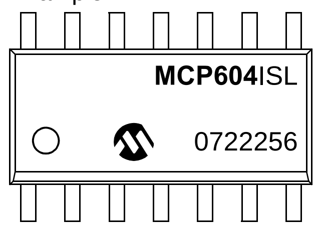
OR



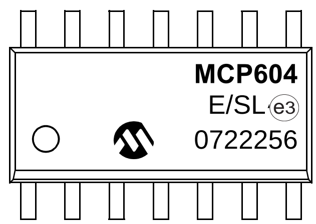
14-Lead SOIC (150 mil) (**MCP604**)



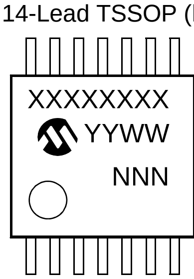
Example:



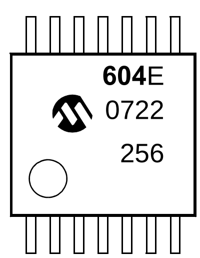
OR



14-Lead TSSOP (**MCP604**)

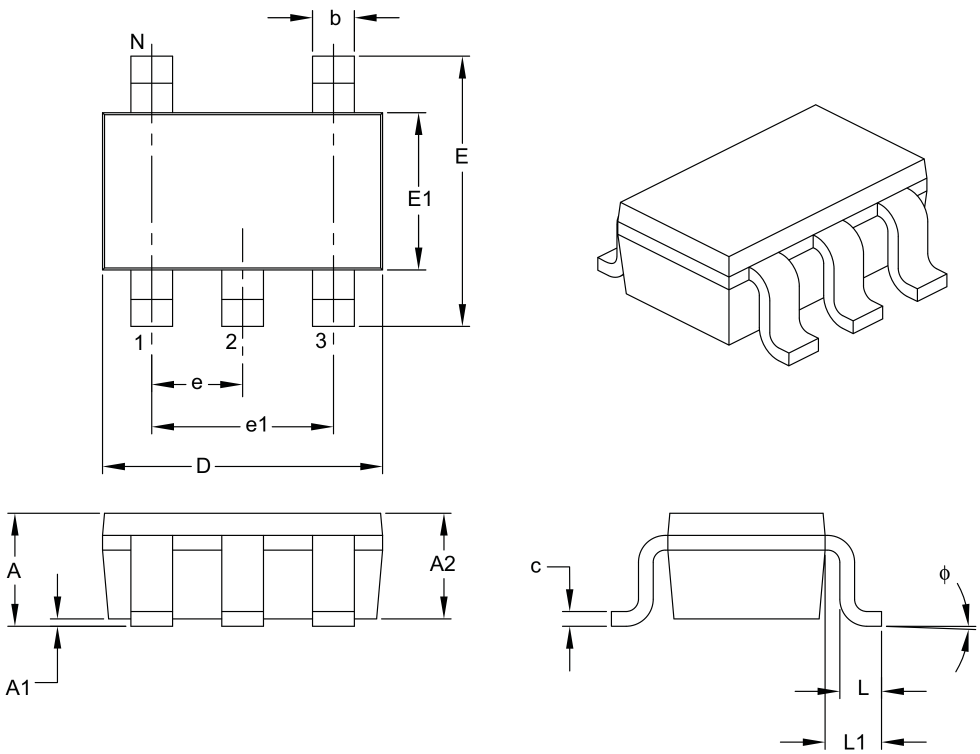


Example:



5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	5		
Lead Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

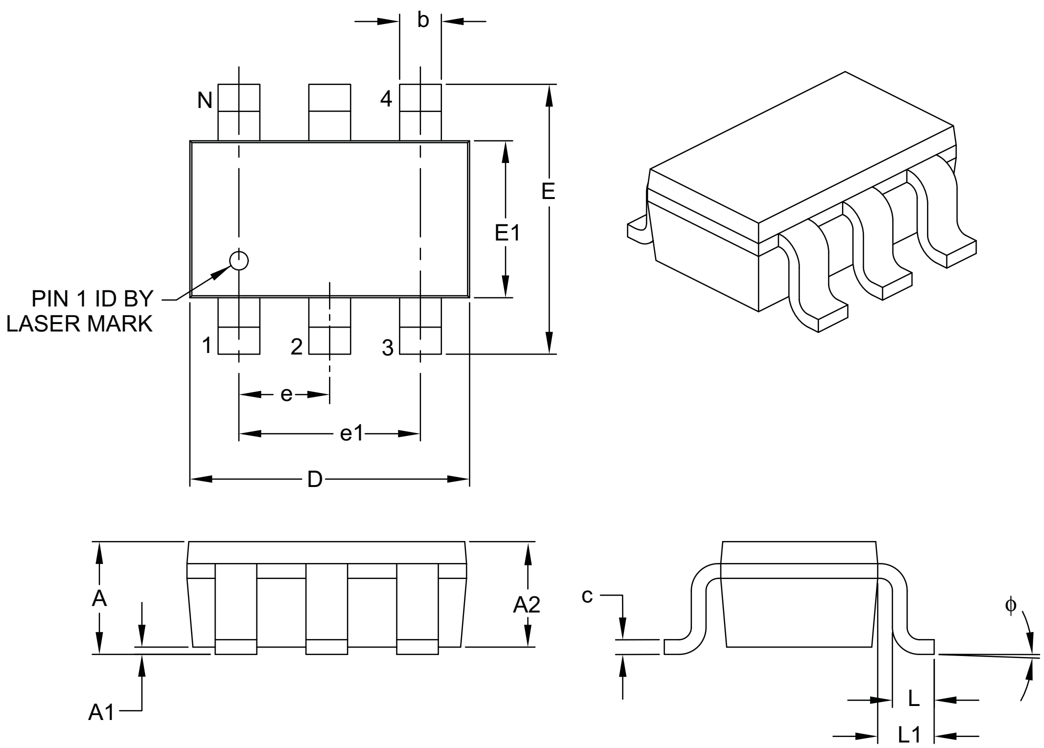
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	φ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

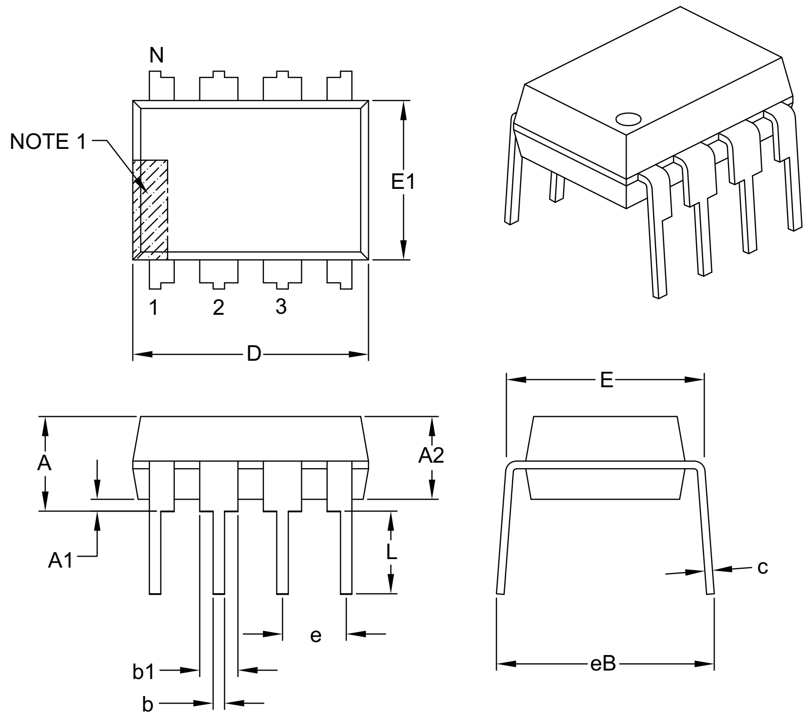
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

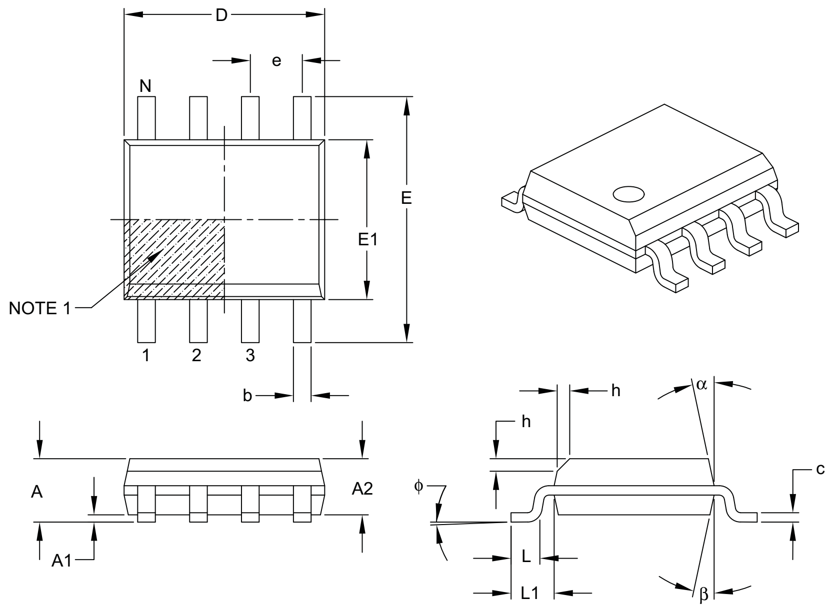
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

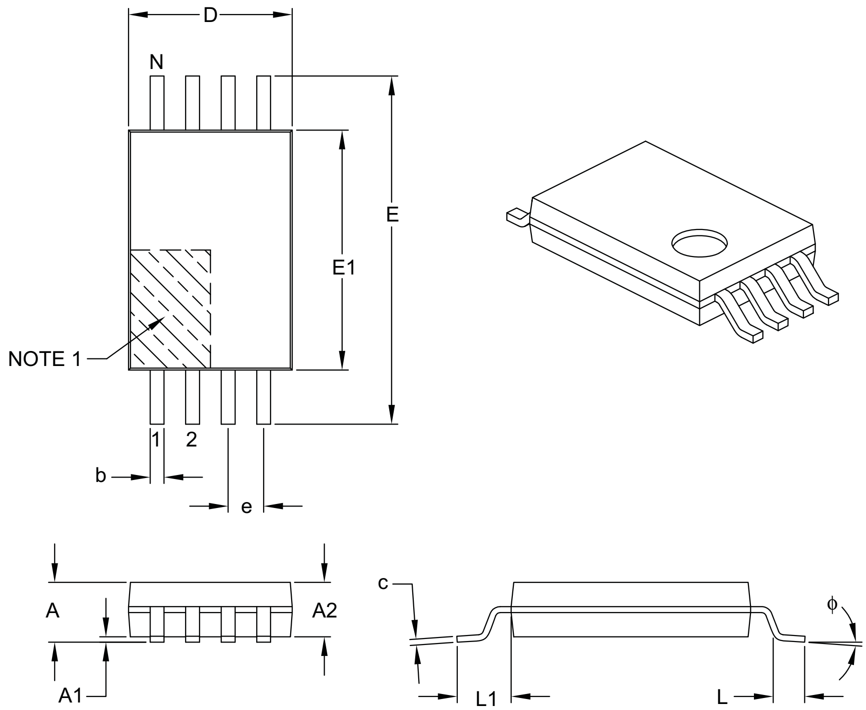
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

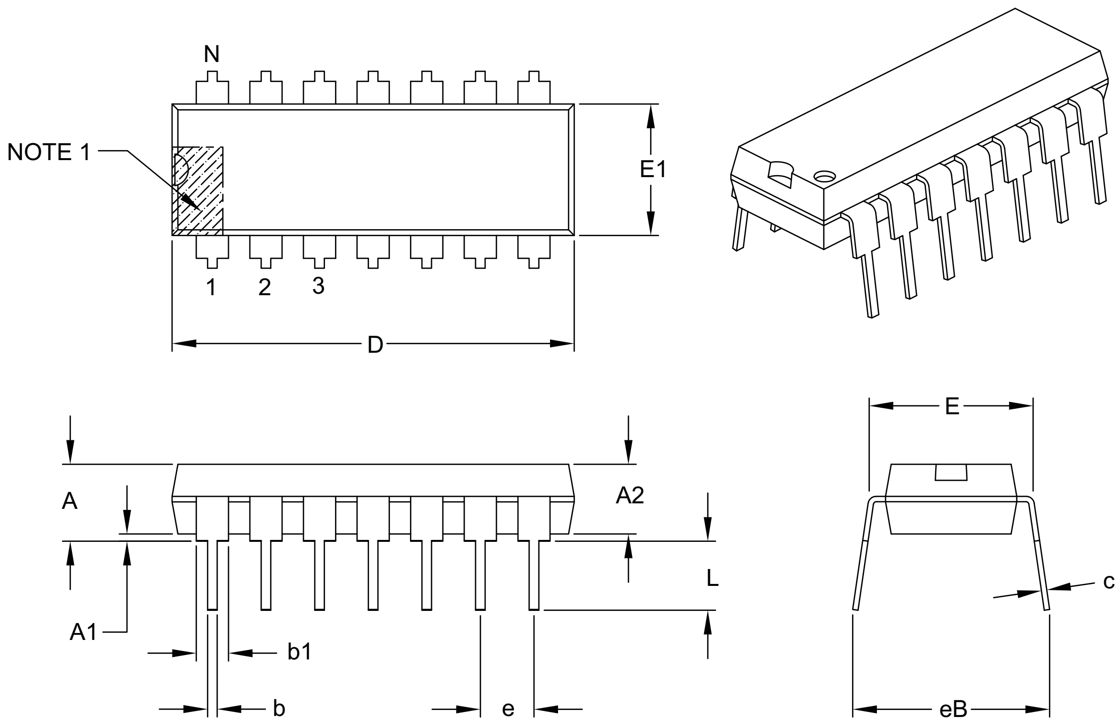
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

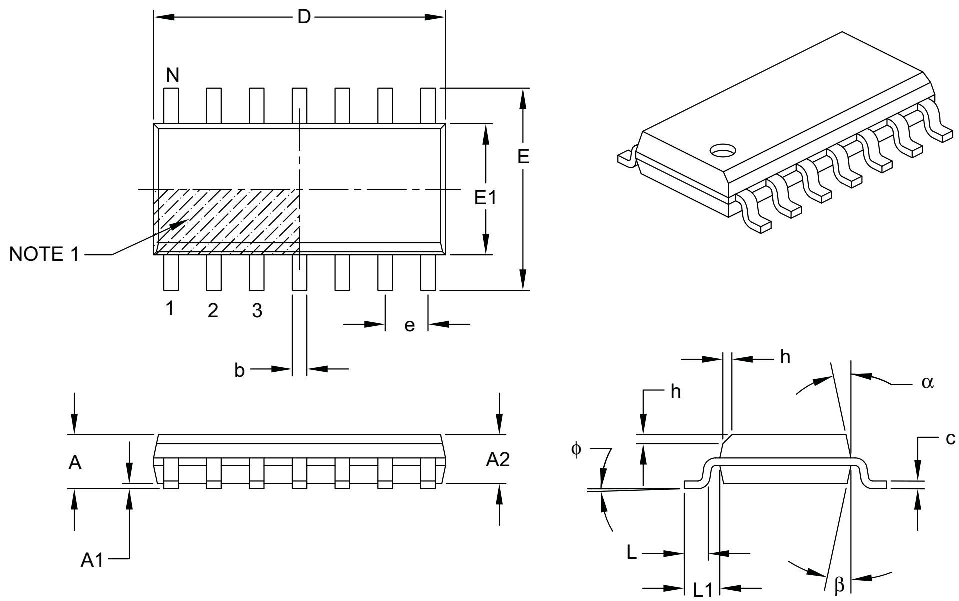
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

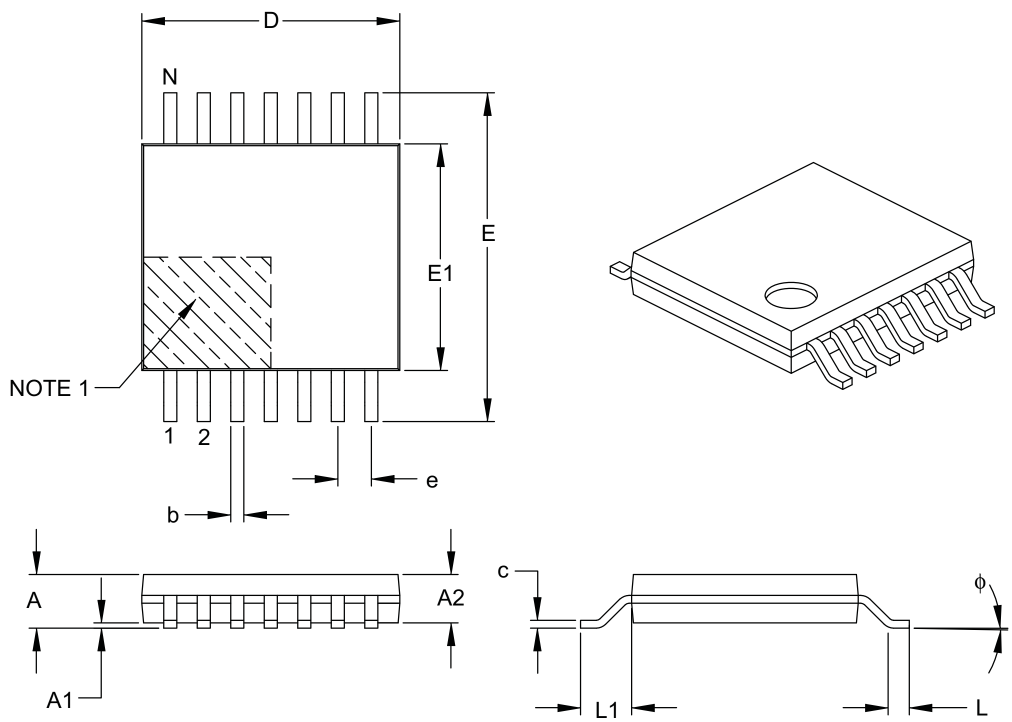
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

NOTES:

APPENDIX A: REVISION HISTORY

Revision G (December 2007)

- Updated Figure 2-15 and Figure 2-19.
- Updated Table 3-1 and Table 3-2.
- Updated notes to **Section 1.0 “Electrical Characteristics”**.
- Expanded Analog Input Absolute Maximum Voltage Range (applies retroactively).
- Expanded operating V_{DD} to a maximum of 6.0V.
- Added Figure 2-34.
- Added **Section 4.1.1 “Phase Reversal”**, **Section 4.1.2 “Input Voltage and Current Limits”**, and **Section 4.1.3 “Normal Operation”**.
- Corrected **Section 6.0 “Packaging Information”**.

Revision F (February 2004)

- Undocumented changes.

Revision E (September 2003)

- Undocumented changes.

Revision D (April 2000)

- Undocumented changes.

Revision C (July 1999)

- Undocumented changes.

Revision B (June 1999)

- Undocumented changes.

Revision A (March 1999)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–X	/XX
Device	Temperature Range	Package

Device	MCP601	Single Op Amp
	MCP601T	Single Op Amp (Tape and Reel for SOT-23, SOIC and TSSOP)
	MCP601RT	Single Op Amp (Tape and Reel for SOT-23-5)
	MCP602	Dual Op Amp
	MCP602T	Dual Op Amp (Tape and Reel for SOIC and TSSOP)
	MCP603	Single Op Amp with Chip Select
	MCP603T	Single Op Amp with Chip Select (Tape and Reel for SOT-23, SOIC and TSSOP)
	MCP604	Quad Op Amp
	MCP604T	Quad Op Amp (Tape and Reel for SOIC and TSSOP)
Temperature Range	I	= -40° C to +85° C
	E	= -40° C to +125° C
Package	OT	= Plastic SOT-23, 5-lead **(MCP601 only)**
	CH	= Plastic SOT-23, 6-lead **(MCP603 only)**
	P	= Plastic DIP (300 mil body), 8, 14 lead
	SN	= Plastic SOIC (3.90 mm body), 8 lead
	SL	= Plastic SOIC (3.90 mm body), 14 lead
	ST	= Plastic TSSOP (4.4 mm body), 8, 14 lead

Examples:

a) MCP601-I/P: Single Op Amp, Industrial Temperature, 8 lead PDIP package.
b) MCP601-E/SN: Single Op Amp, Extended Temperature, 8 lead SOIC package.
c) MCP601T-E/ST: Tape and Reel, Extended Temperature, Single Op Amp, 8 lead TSSOP package
d) MCP601RT-I/OT: Tape and Reel, Industrial Temperature, Single Op Amp, Rotated 5 lead SOT-23 package.
e) MCP601RT-E/OT: Tape and Reel, Extended Temperature, Single Op Amp, Rotated, 5 lead SOT-23 package.

a) MCP602-I/SN: Dual Op Amp, Industrial Temperature, 8 lead SOIC package.
b) MCP602-E/P: Dual Op Amp, Extended Temperature, 8 lead PDIP package.
c) MCP602T-E/ST: Tape and Reel, Extended Temperature, Dual Op Amp, 8 lead TSSOP package.

a) MCP603-I/SN: Industrial Temperature, Single Op Amp with Chip Select, 8 lead SOIC package.
b) MCP603-E/P: Extended Temperature, Single Op Amp with Chip Select, 8 lead PDIP package.
c) MCP603T-E/ST: Tape and Reel, Extended Temperature, Single Op Amp with Chip Select 8 lead TSSOP package.
d) MCP603T-I/SN: Tape and Reel, Industrial Temperature, Single Op Amp with Chip Select, 8 lead SOIC package.

a) MCP604-I/P: Industrial Temperature, Quad Op Amp, 14 lead PDIP package.
b) MCP604-E/SL: Extended Temperature, Quad Op Amp, 14 lead SOIC package.
c) MCP604T-E/ST: Tape and Reel, Extended Temperature, Quad Op Amp, 14 lead TSSOP package.

NOTES:

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